REMARKS

After entry of this amendment, claims 1-29 are pending. In the present Office Action, claim 29 was rejected under 35 U.S.C. § 112, second paragraph. Claims 1-11, 13-21, and 23-29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tran, U.S. Patent No. 6,016,533 ("Tran"). Claims 12 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Wickeraad et al., U.S. Patent No. 6,490,654 ("Wickeraad"). Applicants respectfully traverse these rejections and request reconsideration.

Claims 1-29

Applicants respectfully submit that claims 1-29 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "the memory is configured to output a plurality of values from the set in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory, wherein the cache includes a same number of ways as the memory, and wherein the cache includes a tag memory storing a plurality of tags corresponding to cache lines stored in the cache and a data memory storing the cache lines …the circuit is configured to predict a first way of the plurality of ways to be a hit in the cache for the first address responsive to the first value matching one of the plurality of values, and wherein the first way of the plurality of ways in the memory stores the one of the plurality of values."

Applicants respectfully submit that Tran does not anticipate the above highlighted features. Tran teaches way prediction for a data cache in which a plurality of storage locations store way predictions [Tran, col. 3, lines 20-22], and way predictions are selected from the storage locations based on a first portion of the input address [Tran, col. 3, lines 22-24]. The decoder selects a subset of the memory locations in the cache based on decoding a second portion of the address and the way predictions [Tran, col. 3, lines 25-29]. It is important to note that these memory locations that are selected based on the way predictions and decoding the second portion of the address are not the locations storing the way predictions, but rather are the memory locations that store the cache lines

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themselves. In one embodiment, Tran's decoder selects a subset of the way predictions that were selected based on the first portion of the input address using the second portion of the input address [Tran, col. 3, lines 41-44].

Thus, to summarize, Tran selects way predictions based on a portion of an input address, and uses those way predictions and another portion of the input address to select a cache memory location from which to output data. Nowhere does Tran teach or suggest **predicting a first way to be hit** in the cache for the first address **responsive to the first value matching one of a plurality of values,** wherein the one of the plurality of values is **output from the first way of the memory** as recited in claim 1.

That is, Tran stores way predictions and outputs them to select a cache memory location to output cache data. The stored values are the way predictions. Claim 1 recites storing values in a memory, outputting those values in response to an indication of the first address, and predicting the first way responsive to matching the first value to the plurality of values. Each way prediction in Tran, by contrast, corresponds to a set of cache lines and predicts which way in the set will hit.

Tran also teaches performing tag comparisons to detect a hit in the cache. However, these tag comparisons are not the same as matching the first value to one of the plurality of values. To further highlight this distinction, Applicants have amended claim 1 to explicitly recite the tag memory as part of the cache, and the memory storing the values is separate from that tag memory.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 2-12 depend from claim 1 and recite additional combinations of features not taught or suggested in the cited art. Claims 13 and 23 recite combinations of features including features similar to those highlighted above. Accordingly, claims 13 and 23 are also patentable over the cited art. Claims 14-22 depend from claim 13 and recite additional combinations of features not taught or suggested in the cited art. Claims

24-29 depend from claim 23 and recite additional combinations of features not taught or suggested in the cited art.

Section 112 Rejection

The Office Action noted that the phrase "wherein the circuit is configured to signal the miss the second level cache" in claim 29 was missing one or more transitional words. Applicants have amended claim 29 to recite "wherein the circuit is configured to signal the miss to the second level cache". Applicants respectfully submit that the amendment address the rejection.

The Office Action also stated that claim 29 included the phrase "wherein the second level cache is configured to being an access corresponding to the first address responsive to signal from the circuit" (emphasis added). The Office Action made not further comment on the phrase and did not state what lack of clarity is asserted to exist in the phrase. Applicants respectfully submit that claim 29 recites "wherein the second level cache is configured to begin an access corresponding to the first address responsive to signal from the circuit" (emphasis added). Applicants respectfully submit this phrase is clear.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-97500/LJM.

Respectfully submitted,

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